ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

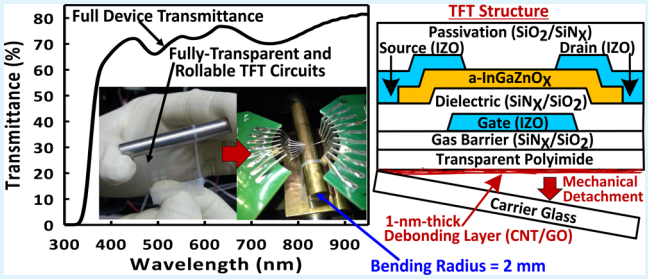
Fully Transparent and Rollable Electronics

Mallory Mativenga, Di Geng, Byungsoon Kim, and Jin Jang*

Advanced Display Research Center, Department of Information Display, Kyung Hee University, 26 kyungheedaero, Dongdaemun-gu, Seoul 130-701, Korea

Supporting Information

ABSTRACT: Major obstacles toward the manufacture of transparent and flexible display screens include the difficulty of finding transparent and flexible semiconductors and electrodes, temperature restrictions of flexible plastic substrates, and bulging or warping of the flexible electronics during processing. Here we report the fabrication and performance of fully transparent and rollable thin-film transistor (TFT) circuits for display applications. The TFTs employ an amorphous indium−gallium−zinc oxide semiconductor (with optical band gap of 3.1 eV) and amorphous indium−zinc oxide transparent conductive electrodes, and are built on 15-μm-thick solution-processed colorless polyimide (CPI), resulting in optical transmittance >70% in the visible range. As the CPI supports processing temperatures >300 °C, TFT performance on plastic is similar to that on glass, with typical field-effect mobility, turn-on voltage, and subthreshold voltage swing of 12.7 ± 0.5 cm^2/V·s, −1.7 ± 0.2 V, and 160 ± 29 mV/dec, respectively. There is no significant degradation after rolling the TFTs 100 times on a cylinder with a radius of 4 mm or when shift registers, each consisting of 40 TFTs, are operated while bent to a radius of 2 mm. For handling purposes, carrier glass is used during fabrication, together with a very thin (∼1 nm) solution-processed carbon nanotube (CNT)/graphene oxide (GO) backbone that is first spin-coated on the glass to decrease adhesion of the CPI to the glass; peel strength of the CPI from glass decreases from 0.43 to 0.10 N/cm, which eases the process of detachment performed after device fabrication. Given that the CNT/GO remains embedded under the CPI after detachment, it minimizes wrinkling and decreases the substrate's tensile elongation from 8.0% to 4.6%. Device performance is also stable under electrostatic discharge exposures up to 10 kV, as electrostatic charge can be released via the conducting CNTs.



KEYWORDS: *transparent, rollable, flexible, thin-film transistor, amorphous oxide semiconductor*

INTRODUCTION

In displays, the combination of transparency and flexibility can have interesting applications—extending beyond displays like embedded windows (for example, in car windshields) or televisions (TVs) that will be invisible when not used. Being transparent, flexible, conformal, and nonbreakable, all at the same time, a transparent and flexible display can be wearable or used as a dynamic paint job in automobiles.[1−6] For a display to be flexible, it should be built on a flexible plastic substrate with flexible components, which is a major challenge, given that plastic substrates cannot withstand the high processing temperatures required to fabricate nondefective semiconductors or dielectrics.[7−10] For the display to be transparent, while being flexible at the same time, all the flexible display components, including the plastic substrate, should also be transparent. Because a large optical band gap (>3 eV) is required for a material to be transparent in the visible range, the choice of nonbrittle and transparent electrodes introduce additional challenges. An electronic device technology that can be fabricated at low temperature or a flexible substrate that can withstand high temperatures is, therefore, required.

Additionally, handling of flexible substrates is an issue because the substrate can shrink, expand, or bulge during fabrication or be stretched, kinked, dimpled, or scratched during unwinding and winding movements.[11,12] These issues lead to loss of layer alignment in the processing and ultimately poor device yield.[12] There are three methods for manufacturing flexible displays on plastic substrates: (1) processing on plastic substrate without using a substrate holder, which is typically used for roll-to-roll technology[13]; (2) fixing a plastic substrate on a glass substrate using adhesive material[14,15]; and (3) coating a polymeric solution on a glass substrate and then detaching the glass later on.[16] The roll-to-roll process is restricted to materials that are solution-processed at low temperatures, while the laminating-type substrate technology suffers from drawbacks such as thermal expansion and thermal damage of adhesive glue. In (3), detachment from glass is very hard and often leads to cracking or wrinkling during the detachment process because the adhesion of the polymer to glass strengthens during device processing. Therefore, there has been considerable research involving the insertion of a release material between the carrier substrate and the flexible substrate.[17−19] However, most of these release layers require lasers for the release process, which are very expensive to install.

Received: October 9, 2014
Accepted: December 19, 2014
Published: December 19, 2014

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

All that being said, there has been very little progress toward the development of displays that are rollable and transparent at the same time. For instance, most of the research on transparent electronics is done on rigid substrates such as glass[20] and most flexible electronics are built with opaque electrodes such as molybdenum (Mo).[21] Some transparent and flexible electronics have, however, been demonstrated but they are not rollable.[22−31] In this paper, we demonstrate fully transparent and rollable amorphous oxide semiconductor (AOS) thin-film transistor (TFT) circuits for the first time. The devices are fabricated on a colorless polyimide (CPI) plastic substrate that is embedded with a thin (∼1 nm) carbon nanotube (CNT)/graphene oxide (GO) backbone. CPI is the substrate of choice because of its higher glass transition temperature, lower coefficient of thermal expansion (CTE), higher chemical resistance, and higher continuous processing temperature compared to other polymer substrates.[32] The CNT/GO backbone and CPI are first spin-coated on carrier glass for mechanical support, followed by device fabrication, and then mechanical detachment from the glass to realize the transparent and rollable circuits. The CNT/GO backbone acts as a debonding layer because it lowers the peel strength of the CPI from glass. Furthermore, the CNT/GO backbone also makes the rollable circuits wrinkle-free because it remains attached to the back side of the CPI after detachment from glass.

MATERIALS AND METHODS

The fully transparent and rollable TFTs presented here employ amorphous indium−gallium−zinc oxide (a-IGZO) as the semiconductor and amorphous indium−zinc oxide (a-IZO) as the transparent conductive electrode. The a-IGZO semiconductor is suitable for transparent electronics because of its large band gap (>3 eV), which makes it transparent in the visible range. Moreover, a-IGZO TFTs exhibit high field-effect mobility (μ_{FE}) and low threshold voltage (V_{TH}), even when the a-IGZO is deposited at room temperature, making them compatible with flexible substrates.[21] The a-IZO is sputter-deposited at room temperature and makes good contact with a-IGZO because both materials are zinc oxide-based. Figure 1 summarizes the fabrication process flow of the fully transparent and rollable circuits.

Substrate Preparation. Thermal and dimensional stability are critical in enabling a film to withstand the high temperatures and/or vacuum conditions required for the deposition of high-quality dielectrics and semiconductors and to ensure precision registration of the different layers in the final device. We, therefore, chose a transparent polymer, CPI, which is one of the high glass transition temperature materials that cannot be melt-processed. Compared with other polymers, it has many advantages, including a low CTE, high chemical resistance, and high continuous processing temperature.[32]

Glass is used as the carrier substrate on which the CPI is spin-coated. Before coating the glass with CPI, however, a mixture of CNT and GO is first deposited on the glass. The summary of the fabrication process is presented in Figure 1. First, a mixture of water-based CNT solution, Unidym Carbon Nanotubes, and GO solution is spin-coated on top of the carrier glass to a thickness ranging from 0.7 to 1 nm. The GO solution is acquired from the Graphene Supermarket. The CNT/GO solution is spin-coated for 25 s at 500 rotations per minute (rpm) followed by subsequent baking at 250 °C in an oven. The CPI is then spin-coated at 1000 rpm to achieve a

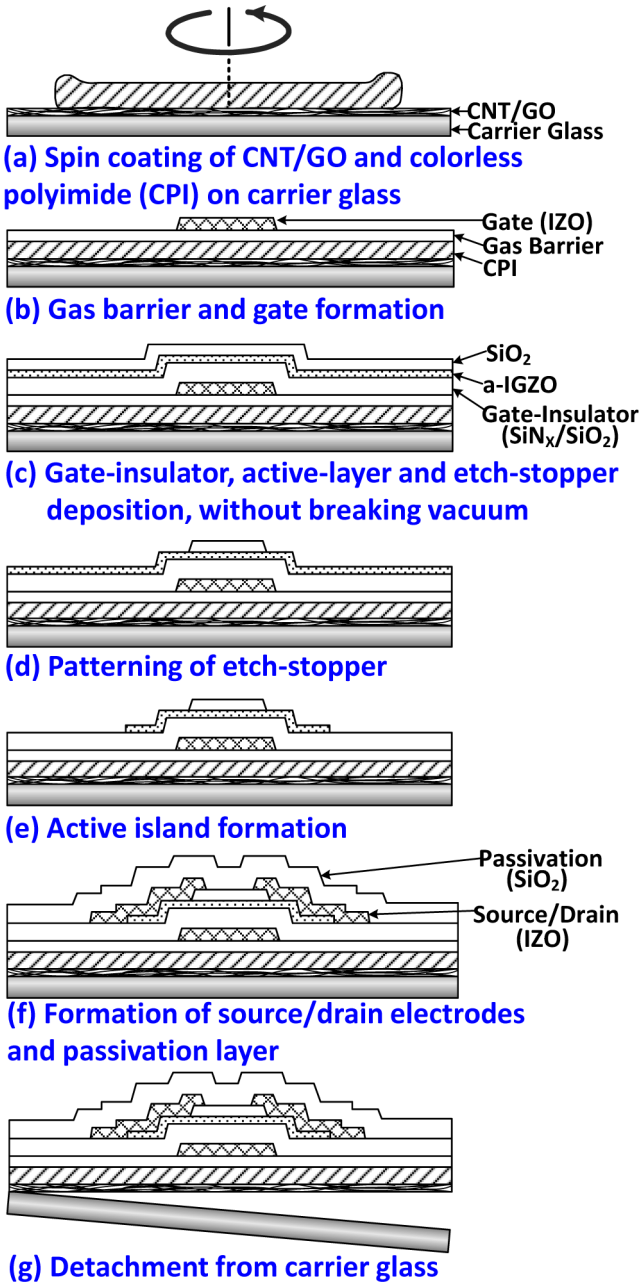


Figure 1. Fabrication process flow of fully transparent and rollable a-IGZO TFT circuits.

thickness around 15 μm (Figure 1a). An additional baking of the glass/CNT/GO/CPI substrates is carried out at 320 °C in an oven.

TFT Fabrication. After the formation of the CNT/GO backbone and CPI film on the carrier glass, the fabrication of the a-IGZO TFTs is initiated by the deposition of a stack of alternate SiO_2 and SiN_x layers (five layers in total starting with SiO_2) with thickness of 25 nm each at 300 °C by plasma-enhanced chemical vapor deposition (PECVD) to form a buffer layer, which acts as a gas barrier (less than 10^{-3} g/d·m^2). A 60 nm thick, IZO layer is deposited on top of the buffer layer by sputtering at room temperature and patterned to form the gate electrode (Figure 1b). This is followed by the consecutive deposition of a 200 nm thick SiO_2 layer by PECVD at 300 °C as the gate insulator, a 20 nm thick a-IGZO layer by direct current (dc) sputtering at 200 °C, and a 100 nm thick SiO_2

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

layer by PECVD at 200 °C, in a cluster deposition tool, without breaking vacuum (Figure 1c). The top SiO_2 layer, commonly referred to as "etch stopper", protects the a-IGZO from exposure to air and also shields it from being etched away or contaminated by the etchant used to define the source/drain electrodes. For the a-IGZO layer deposition, a polycrystalline IGZO target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol %) is used and the sputtering is done in an Ar and O_2 gas mixture (Ar:O_2 ratio = 4:16 sccm).

After patterning the etch stopper by dry etching in a mixture of NF_3 and H_2 (Figure 1d), the a-IGZO is patterned by an indium tin oxide (ITO) etchant to form the active island (Figure 1e). A 150 nm thick IZO layer is deposited by sputtering at room temperature and patterned as the source/drain electrode. Then a 200 nm thick SiO_2 layer is deposited by PECVD at 200 °C as the passivation layer (Figure 1f) and an annealing process is carried out at 250 °C in vacuum to ensure a reproducible unstressed state. Finally, the PI substrate is mechanically detached from the glass to realize the flexible electronics (Figure 1g).

Device Characterization. The Agilent 4156C precision semiconductor parameter analyzer is used to monitor all electrical measurements. TFTs' current−voltage characteristics are measured in dark and at room temperature. The TFT's turn-on voltage (V_{ON}) is taken as the gate voltage (V_{GS}) at which the drain current (I_{DS}), measured with drain voltage (V_{DS}) = 0.1 V, starts to monotonically increase. The field-effect mobility (μ_{FE}), derived from transconductance (g_M), $\partial I_{DS}/\partial V_{GS}$, is given by $\mu_{FE} = (g_M L)/(W V_{DS} C_{OX})$, where C_{OX} is the gate-insulator capacitance per unit area and V_{DS} = 0.1 V. The subthreshold swing (SS) is taken as $(\mathrm{d}\log(I_{DS})/\mathrm{d}V_{GS})^{-1}$ of the range 10 pA ≤ I_{DS} ≤ 100 pA, with V_{DS} = 0.1 V.

The tensile strength and tensile elongation of the CPI substrate were recorded at a drawing rate of 500 mm/min with sample dimensions of 100 mm in length and 5 mm in width (test method: ASTM D638-107). Tape peel strength evaluation was used to measure the peel strength of the CPI from glass with a speed of 50 mm/min and extension of 20 mm.

RESULTS AND DISCUSSION

Effect of CNT/GO Backbone. Because of the weak adhesion of the CNT/GO backbone to the carrier glass, detachment from carrier glass is achieved by applying a small amount of force. After detachment from the carrier glass, the CNT/GO backbone remains embedded under the CPI substrate, without any residue left on the glass. An atomic force microscope (AFM) image of the back side of the CPI substrate with the CNT/GO backbone is taken to investigate the surface morphology of the CNT/GO/CPI substrate (Figure 2b). A root-mean-square (RMS) roughness of the backside of the plastic substrate is ∼2.9 nm and the GO particles are in the range of 1−3 μm with thicknesses varying from 0.5 to 1.25 nm. Peel strength of the CPI from carrier glass decreases from 0.43 to 0.10 N/cm by inserting the CNT/GO backbone. Having a flakelike structure with CNT links, the CNT/GO layer decreases the area where the CPI contacts the glass, thereby reducing its adhesion to glass. Both CNT and GO are hydrophobic and either can be used as a debonding layer. However, mixing the two gives a denser layer and smoother surface. Being denser, the CNT/GO backbone further eases the detachment process and its smoother surface further reduces stress in the plastic substrate.

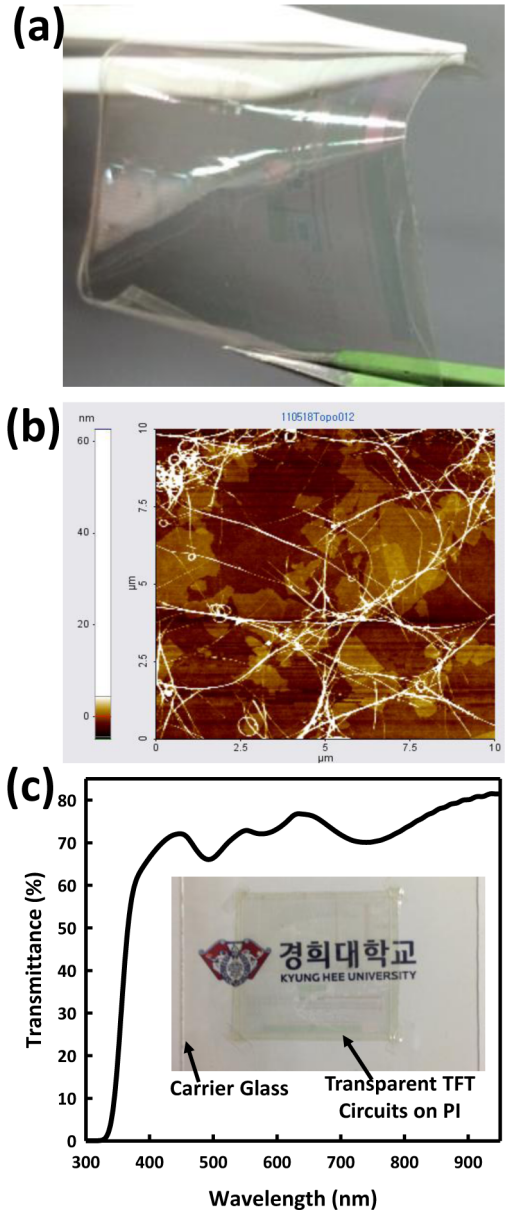


Figure 2. Fully transparent and rollable circuits: (a) Image of fabricated fully transparent and rollable a-IGZO TFT circuits after detachment from carrier glass; (b) atomic force microscope (AFM) image obtained from the backside of the CPI substrate with the CNT/GO backbone; (c) optical transmittance of the a-IGZO TFT circuits. Inset shows transparency of the rollable a-IGZO TFT devices attached to a carrier glass.

Owing to the embedded CNT/GO backbone, the tensile strength of the CPI substrate increases from 238 to 247 MPa, while its tensile elongation decreases from 8% to 4.6%. Tensile strength is the maximum stress that a material can withstand while being stretched or pulled before failing or breaking, whereas tensile elongation is the percentage increase in length that occurs before it breaks under tension. Therefore, a combination of high tensile strength and low tensile elongation is an indication of high robustness of the CPI substrate. Furthermore, it is seen that the existence of the CNT/GO backbone minimizes electrostatic discharge (ESD) damage, as it may aid in the release of localized ESD. Given the insulating properties of the glass/PI substrate, it is easy to have charge

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

buildup in the devices. However, when the PI is embedded with CNT/GO, electrostatic charge can be released via the conductive CNT in the CNT/GO backbone. Therefore, the uniqueness of this substrate lies in the fact that the CNT/GO stack layer is also detached along with the PI substrate, without any residue left on the carrier glass. This method is, therefore, completely different from the debonding layer (DBL) methods by other groups, such as ITRI (Industrial Technology Research Institute), Taiwan, in which the DBL remains on the glass.[33] Given that only a thickness of ~1 nm is required, the cost of inserting the CNT/GO backbone is very low.

Performance of the Fully Transparent and Rollable a-IGZO TFTs. Optical transmittance of the full TFT devices is measured to be ~70% in the visible range (Figure 2c). Figure 3a is an optical image of a fabricated TFT. Layer thicknesses were verified by high-resolution transmission electron microscope (TEM) images and found to be very close to the targeted thicknesses (Figure 3b). Several TFTs were measured and characterized to obtain the mean and standard deviations of critical TFT parameters, before and after detachment from glass. Parts (c) and (d) of Figure 3 show respectively typical transfer characteristics and output characteristics of the rollable and transparent a-IGZO TFTs, before and after detachment from glass. It is interesting to note that there is no significant degradation of TFT parameters after detachment from glass, which indicates the reliability of the release method. The off-state leakage currents are lower than the measurement limit, before and after detachment from glass (Figure 3c). Output characteristics measured at very low V_{DS} show no current crowding (Figure 3d, blowup), which is an indication of a good contact between IZO and a-IGZO. TFT parameters, extracted before and after detachment from glass, are summarized in Table 1.

After detachment from carrier glass, the μ_{FE} slightly increases (from 12.5 ± 34 to 12.7 ± 46 $cm^2/V{\cdot}s$), V_{ON} slightly shifts to the negative V_{GS} direction (from −1.5 ± 0.33 to 1.7 ± 0.17 V), and SS slightly increases (from 156 ± 14 to 160 ± 29 mV/dec). The changes in TFT parameters after detachment may be related to the mechanical strain during the detach process. Channel conductivity may increase after the application of mechanical strain to the TFT, which may result in an increase in μ_{FE} and a negative shift of V_{ON} after detachment.[30,34]

Rolling Test. A rolling test was performed to test the mechanical flexibility of the TFTs. The rolling test was carried out by rolling the samples on a cylinder with radius R = 4 mm. An automated rolling machine, specifically designed for this purpose, was used (Figure 4a). As the rolling machine repetitively moves back and forth, the attached sample is repeatedly rolled and reflated (see video provided as Supporting Information). The placement of the sample on the cylinder is such that the direction of the rolling stress is perpendicular to the flow of the I_{DS}. The external rolling force is applied up to 100 times (Figure 4b). The difference in the coefficients of TFT layers, and the built-in strain during buffer layer deposition, may cause the as-fabricated TFTs to be under tensile strain, which is the reason why samples may curl after detachment from glass (Figure 2a). Therefore, both the fabrication process and the externally applied bending moment cause strain in the TFTs fabricated on plastic substrates. However, these TFTs could be rolled up to 100 times, without significant degradation, which indicates robustness of these fully transparent and rollable a-IGZO TFTs (Figure 4b).

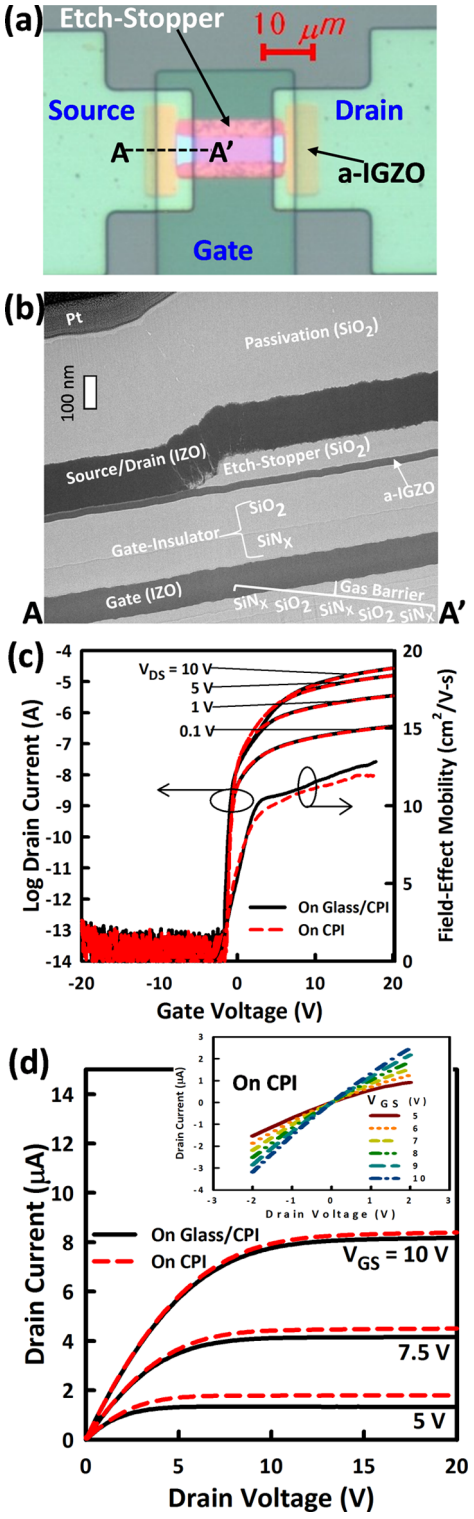


Figure 3. Structure and operation of the fully transparent rollable a-IGZO TFTs before and after detachment from glass: (a) Optical micrograph of a fabricated fully transparent and rollable a-IGZO TFT; (b) transmission electron microscope (TEM) image of the cross section through the dashed line AA′ in (a); (c) transfer characteristics and field-effect mobility; (d) output characteristics. Blow-up image is a magnified version of the output characteristics for drain voltages close to 0 V, showing good ohmic contacts between IZO and a-IGZO. The TFT channel width (W) = 10 μm and channel length (L) = 20 μm.

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

Table 1. TFT Parameters, Measured before and after Detachment from Carrier Glass

	before detachment (on glass/CPI)		after detachment (on CPI)	
	mean	standard deviation	mean	standard deviation
μ_{FE}[a] (cm^2/V·s)	12.50	0.34	12.70	0.46
V_{ON}[b] (V)	−1.50	0.33	−1.74	0.17
SS[c] (mV/dec)	156	14	160	29

[a]μ_{FE}: Field-effect mobility. [b]V_{ON}: Turn-on voltage. [c]SS: Subthreshold-voltage swing.

Electrostatic Discharge (ESD) Test. The samples were exposed to an ionized air gun with voltages varying from 1 to 10 kV. ESD is a major reliability issue for TFTs, especially those on plastic substrates, given that plastic is usually associated with the generation of electrostatic charge. Under electrostatic discharge exposures of up to 10 kV, the TFTs on the PI substrate embedded with the CNT/GO backbone exhibit better stability in terms of V_{ON} and off-current levels compared to those on the PI substrate without the CNT/GO backbone (Figure 5). This indicates that the CNT/GO layer on the back side of the PI releases the localized ESD via the conductive CNT. Sheet resistance of ∼259 kΩ is measured at the back side of the CPI substrate after detachment. Apart from the improvement of the TFT's stability under ESD and the mechanical support it provides to the plastic substrate, the CNT/GO backbone impose no additional effects on TFT performance.

Integrated Circuits. For flexible display applications, driver circuits should be integrated on the TFT backplane as the use of rigid external driver circuits limit the display flexibility. We, therefore, demonstrate here the performance of a fully transparent rollable shift register (gate driver). The shift register has a 40 μm pitch, which is attractive for high-resolution displays. Its schematic design and timing diagram are depicted in Figure 6a. The detailed operation of this shift register was presented elsewhere.[35] A single-stage circuit consists of five TFTs (T1−T5) and one bootstrap capacitor (C). T1 and T3 are respectively the input and driving TFTs, while T2 and T4 are the low-level holding unit. T5 serves as a suppressor of the feed-through effect. This shift register design employs nonoverlapping two-phase clock signals (CLK1 and CLK2) for the timing and shifting of the input signal. The L of all TFTs is 9 μm and the W values are different as determined experimentally for optimum performance.[35] Figure 6b shows the optical image of the fabricated fully transparent and rollable eight-stages shift register. One single stage occupies a small area of 646 μm × 40 μm, given that the bootstrap capacitor is only 0.5 pF and T3, the largest TFT, has W = 400 μm. The shift register is, therefore, compatible with narrow bezel active matrix displays.

Samples were wound around rods with different diameters and measured while being bent (Figure 6c). Measurements were successfully performed on rods with a radius of 2 mm, without significant distortion of the shift-register's output waveform. As the side with the TFTs was facing upward, the TFTs were under tensile strain when wound to the rod with the radius of 2 mm. Parts (d) and (e) of Figure 6 show respectively the output waveform of the first and last stages of the 40 μm pitch shift register. For input V_{DD} of 20 V, a clock frequency of 166.7 kHz was used, which corresponds to a pulse width of 3 μs. For the first stage, the high-output voltage and rise and fall times were respectively ∼19.7 V and 0.9 and 0.8 μs. For the last

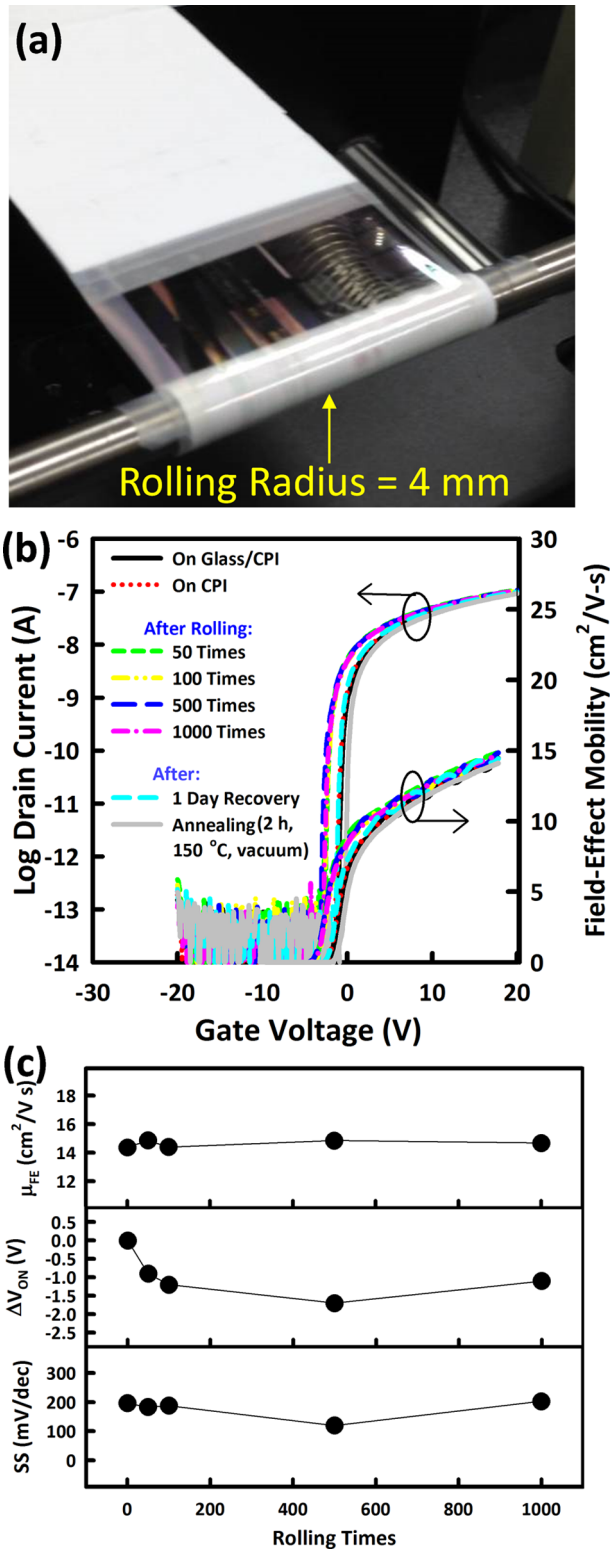


Figure 4. Operation of the fully transparent rollable a-IGZO TFTs after rolling to a cylinder with radius R = 4 mm: (a) Image of sample as it is being rolled to the cylinder; (b) transfer characteristics before and after rolling for incremental times with V_{DS} = 0.1 V. Evolution of the fully transparent rollable a-IGZO TFT parameters after rolling to a cylinder with radius R = 4 mm: The TFT channel width (W) = 10 μm and channel length (L) = 20 μm.

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

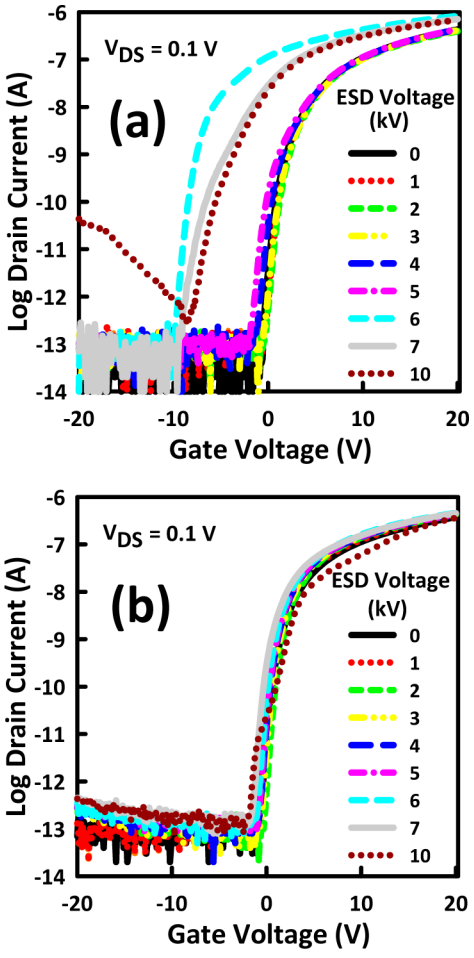


Figure 5. Effect of electrostatic discharge (ESD) on fully transparent and rollable a-IGZO TFTs (a) without and (b) with the CNT/GO backbone. The TFT channel width (W) = 10 μm and channel length (L) = 10 μm.

stage, the high-output voltage was still 19.7 V, but the rise and fall times increased slightly to 1.3 and 1.0 μs, respectively. These results indicate high flexibility of the fully transparent and rollable TFT circuits and hence the possibility of their application to rollable and transparent displays, as bending to small radii has virtually negligible effect on their performance. The slight difference in the first and last outputs of the SRs are an indication that all 40 TFTs in each SR are stable under bending radius of 2 mm. Stability at even smaller bending radius is possible, but not easy to test, given the hardness of the probe contacting TFT circuits at bending radii <2 mm.

SUMMARY

In summary, fully transparent and rollable AOS TFT circuits are demonstrated for the first time. The uniqueness of the substrate lies in the existence of a CNT/GO backbone that is embedded to the back side of the CPI. This backbone facilitates the detachment process from carrier glass, provides mechanical support to the CPI, and also acts a pathway for ESD discharge. Transmittance of 70% is achieved for the full circuit devices and the contact between the a-IGZO and the transparent conductive electrode (IZO) has been shown to be close to ohmic, resulting in good device scaling. Devices could be rolled 100 times on a cylinder with radius of 4 mm, without significantly degrading their performance, and integrated

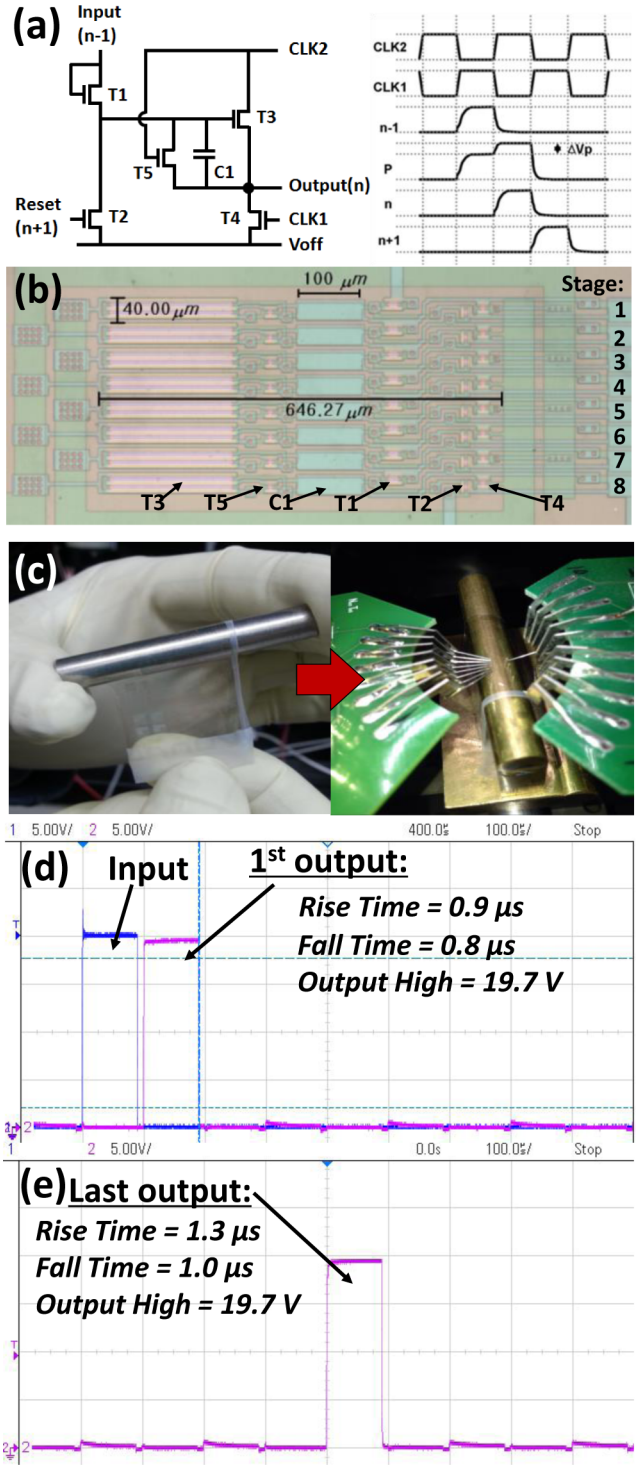


Figure 6. Operation of a fully transparent and rollable a-IGZO TFT shift register (SR): (a) One stage circuit schematic and timing diagram of the two-clock, five transistor (5T), and one capacitor (1C) SR; (b) optical micrograph of a measured eight-staes SR; (c) image of the sample containing the SR as it being rolled to a cylinder and the measurement setup for the SR, while under bending stress. (d and e) First output and last output of the eight-stage SR under bending radius of 2 mm for input voltage V_{DD} = 20 V.

circuits also operated without degradation, while being bent to a radius of 2 mm, making these devices suitable for transparent and rollable displays.

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

■ ASSOCIATED CONTENT

Supporting Information

Rolling test video. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*Telephone: +82-2-961-9153. Fax: +82-2-961-9154. E-mail: jjang@khu.ac.kr.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the Industrial Strategic Technology Development Program (10045269, Development of Soluble TFT and Pixel Formation Materials/Process Technologies for AMOLED TV) funded by MOTIE/KEIT.

■ REFERENCES

(1) Thomas, G. Invisible Circuits. *Nature (London, U. K.)* **1997**, *389*, 907−908.

(2) Wager, J. F. Transparent Electronics. *Science (Washington, DC, U. S.)* **2003**, *300*, 1245−1246.

(3) Someya, T.; Sekitani, T.; Iba, S.; Kato, Y.; Kawaguchi, H.; Sakurai, T. A. Large-Area, Flexible Pressure Sensor Matrix with Organic Field-Effect Transistors for Artificial Skin Applications. *Proc. Natl. Acad. Sci. U. S. A.* **2004**, *101*, 9966−9970.

(4) Forrest, S. R. The Path to Ubiquitous and Low-Cost Organic Electronic Appliances on Plastic. *Nature (London, U. K.)* **2004**, *428*, 911−918.

(5) Lim, H. C.; Schulkin, B.; Pulickal, M. J.; Liu, S.; Petrova, R.; Thomas, G.; Wagner, S.; Sidhu, K.; Federici, J. F. Flexible Membrane Pressure Sensor. *Sens. Actuators, A* **2005**, *119*, 332−335.

(6) Reuss, R. H.; Chalamala, B. R.; Moussessian, A.; Kane, M. G.; Kumar, A.; Zhang, D. C.; Rogers, J. A.; Hatalis, M.; Temple, D.; Moddel, G.; Eliasson, B. J.; Estes, M. J.; Kunze, J.; Handy, E. S.; Harmon, E. S.; Salzman, D. B.; Woodall, J. M.; Alam, M. A.; Murthy, J. Y.; Jacobsen, S. C.; Olivier, M.; Markus, D.; Campbell, P. M.; Snow, E. Macroelectronics: Perspectives on Technology and Applications. *Proc. IEEE* **2005**, *93*, 1239−1256.

(7) Park, J. S.; Kim, T. W.; Stryakhilev, D.; Lee, J. S.; An, S. G.; Pyo, Y. S.; Lee, D. B.; Mo, Y. G.; Jin, D. U.; Chung, H. K. Flexible Full Color Organic Light-Emitting Diode Display on Polyimide Plastic Substrate Driven by Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors. *Appl. Phys. Lett.* **2009**, *95*, 013503-1−013503-3.

(8) Miura, K.; Ueda, T.; Nakano, S.; Saito, N.; Hara, Y.; Sugi, K.; Sakano, T.; Yamaguchi, H.; Amemiya, I. Low-Temperature-Processed IGZO TFTs for Flexible AMOLED with Integrated Gate Driver Circuits. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2011**, *42*, 21−24.

(9) Jin, D. U.; Kim, T. W.; Koo, H. W.; Stryakhilev, D.; Kim, H. S.; Seo, S. J.; Kim, M. J.; Min, H. K.; Chung, H. K.; Kim, S. S. Highly Robust Flexible AMOLED Display on Plastic Substrate with New Structure. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2010**, *41*, 703−705.

(10) Nakata, M.; Sato, H.; Nakajima, Y.; Fujisaki, Y.; Takei, T.; Shimizu, T.; Suzuki, M.; Fukagawa, H.; Motomura, G.; Yamamoto, T.; Fujikake, H. 16.4: Low-Temperature Fabrication of Flexible AMOLED Displays Using Oxide TFTs with Polymer Gate Insulators. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2011**, *42*, 202−205.

(11) Nisato, G. Koninklijke Philips Electronics. *NL*, Flexible Devices. 048669, May 26, 2005.

(12) Jain, K.; Klosner, M.; Zemel, M.; Raghunandan, S. Flexible Electronics and Displays: High-Resolution, Roll-to-Roll, Projection Lithography and Photoablation Processing Technologies for High-Throughput Production. *Proc. IEEE* **2005**, *93*, 1500−1510.

(13) Yeh, Y.-H; Cheng, C.-C.; Lai, B. C.-M.; Leu, C.-M.; Tseng, Y.-L. Flexible Hybrid Substrates of Roll-to-Roll Manufacturing for Flexible Display Application. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2013**, *21*, 34−40.

(14) Haq, J.; Ageno, S.; Raupp, G. B.; Vogt, B. D.; Loy, D. Temporary Bond-Debond Process for Manufacture of Flexible Electronics: Impact of Adhesive and Carrier Properties on Performance. *J. Appl. Phys. (Melville, NY, U. S.)* **2010**, *108*, 114917-1−114917-7.

(15) O'Rourke, S. M.; Loy, D. E.; Moyer, C.; Bawolek, E. J.; Ageno, S. K.; O'Brien, B. P.; Marrs, M.; Bottesch, D.; Dailey, J.; Naujokaitis, R.; Kaminski, J. P.; Allee, D. R.; Venugopal, S. M.; Haq, J.; Colaneri, N.; Raupp, G. B.; Morton, D. C.; Forsythe, E. W. Direct Fabrication of a-Si:H Thin Film Transistor Arrays on Plastic and Metal Foils for Flexible Displays. *Proc. 26th Army Sci. Conf., Orlando, FL* **2008**, 1−5.

(16) Jang, J.; Choi, M. H.; Kim, B. S.; Lee, W. G.; Seok, M. J.; Ryu, D.-S. Robust TFT Backplane for Flexible AMOLED. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2012**, *43*, 260−263.

(17) Lee, C.-C.; Hang, Y.-Y.; Cheng, H.-C.; Ho, J.-C.; Chen, J. A Novel Approach to Make Flexible Active Matrix Displays. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2010**, *41*, 810−813.

(18) French, I.; McCulloch, D.; Boerefijn, I.; Kooyman, N. Thin Plastic Electrophoretic Displays Fabricated by a Novel Process. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2005**, *36*, 1634−1637.

(19) Cai, J.; Han, D.; Geng, Y.; Wang, W.; Wang, L.; Zhang, S.; Wang, Y. High-Performance Transparent AZO TFTs Fabricated on Glass Substrate. *IEEE Trans. Electron Devices* **2013**, *60*, 2432−2435.

(20) Park, S.-H. K.; Ryu, M.; Yang, S.; Byun, C.; Hwang, C.-S.; Cho, K. I.; Im, W.-B.; Kim, Y.-E.; Kim, T.-S.; Ha, Y.-B.; Kim, K.-B. Oxide TFT Driving Transparent AM-OLED. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2010**, *41*, 245−248.

(21) Mativenga, M.; Choi, M. H.; Choi, J. W.; Jang, J. Transparent Flexible Circuits Based on Amorphous-Indium−Gallium−Zinc−Oxide Thin-Film Transistors. *IEEE Electron Device Lett.* **2011**, *32*, 170−172.

(22) Nomura, K.; Ohta, H.; Ueda, K.; Kamiya, T.; Hirano, M.; Hosono, H. Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor. *Science (Washington, DC, U. S.)* **2003**, *300*, 1269−1272.

(23) Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors. *Nature (London, U. K.)* **2004**, *432*, 488−492.

(24) Fortunato, E.; Barquinha, P.; Pimentel, A.; Goncalves, A.; Marques, A.; Pereira, L.; Martins, R. Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature. *Adv. Mater. (Weinheim, Ger.)* **2005**, *17*, 590−595.

(25) Mamazza, R.; Morel, D. L.; Ferekides, C. S. Transparent Conducting Oxide Thin Films of Cd_2SnO_4 Prepared by RF Magnetron Co-sputtering of the Constituent Binary Oxides. *Thin Solid Films* **2005**, *484*, 26−33.

(26) Ong, C. W.; Zong, D. G.; Aravind, M.; Choy, C. L. Tensile Strength of Zinc Oxide Films Measured by a Microbridge Method. *J. Mater. Res.* **2003**, *18*, 2464−2472.

(27) Leterrier, Y.; Medico, L.; Demarco, F.; Manson, J.-A. E.; Betz, U.; Escola, M. F.; K. Olsson, M. K.; Atamny, F. Mechanical Integrity of Transparent Conductive Oxide Films for Flexible Polymer-Based Displays. *Thin Solid Films* **2004**, *460*, 156−166.

(28) Liu, J.-M.; Lee, T. M.; Wen, C.-H.; Leu, C.-M. High-Performance Organic−Inorganic Hybrid Plastic Substrate for Flexible Displays and Electronics. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2012**, *19*, 63−69.

(29) Nomoto, K.; Noda, M.; Kobayashi, N.; Katsuhara, M.; Yumoto, A.; Ushikura, S.; Yasuda, R.; Hirai, N.; Yukawa, G.; Yahi, I. Rollable OLED Display Driven by Organic TFTs. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2011**, *42*, 488−491.

(30) Zhou, J.; Wu, G.; Guo, L.; Zhu, L.; Wan, Q. Flexible Transparent Junctionless TFTs with Oxygen-Tuned Indium-Zinc-Oxide Channels. *IEEE Electron Device Lett.* **2013**, *34*, 888−890.

(31) Jiang, J.; Sun, J.; lu, A.; Wan, Q. Self-Assembled Ultralow-Voltage Flexible Transparent Thin-Film Transistors Gated by SiO_2-

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585

Based Solid Electrolyte. *IEEE Trans. Electron Devices* **2011**, *58*, 547−549.
(32) Takenobu, T.; Takahashi, T.; Kanbara, T.; Tsukagoshi, K.; Aoyagi, Y.; Iwasa, Y. High-Performance Transparent Flexible Transistors using Carbon Nanotube Films. *Appl. Phys. Lett.* **2006**, *88*, 033511-1−033511-3.
(33) Chien, C. W.; Wu, C. H.; Tsai, Y. Y.; Kung, Y. C.; Lin, C. Y.; Hsu, P. C.; Hsieh, H. H.; Wu, C. C.; Yeh, Y. H.; Leu, C. M.; Lee, T. M. High-performance Flexible a-IGZO TFTs Adopting Stacked Electrodes and Transparent Polyimide-Based Nanocomposite Substrates. *IEEE Trans. Electron Devices* **2011**, *58*, 1440−1446.
(34) Münzenrieder, N.; Cherenack, K. H.; Tröster, G. The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs. *IEEE Trans. Electron Devices* **2011**, *50*, 2041−2048.
(35) Geng, D.; Kim, B. S.; Mativenga, M.; Seok, M. J.; Kang, D. H.; Jang, J. 40 um-pitch IGZO TFT Gate Driver for High-resolution Rollable AMOLED. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* **2013**, *44*, 927−930.

DOI: 10.1021/am506937s
ACS Appl. Mater. Interfaces 2015, 7, 1578−1585